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14. ABSTRACT
During the project period, phorsphorene field-effect transistors (FETs) were successfully passivated with atomic-layer-deposited Al2O3 and proven to be stable for at least three months in room air. Meanwhile, the FET design evolved from long back-gated channels on conducting substrates that could be assessed only under direct-current conditions, to submicron top-gated channels that could operate at microwave frequencies under both small-signal and large-signal conditions. Further, CMOS-compatible submicron buried-gate structures were designed. However, lacking large-area phosphorene layers, the design was demonstrated only on monolayer MoS2 grown by chemical vapor deposition.

15. SUBJECT TERMS
Elemental semiconductors, high-k gate dielectrics, semiconductor-insulator interfaces, thermal stability, two-dimensional hole gas

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Accomplishments

What were the major goals and objectives of the project?

The objective of the proposed research is to assess the potential of phosphorene, a two-dimensional (2D) atomic layer of black phosphorus, for overcoming the limitations of all other 2D and three-dimensional materials for high-speed and high-frequency transistors thereby transforming the electronics industry. To this end, transistor test structures would initially be fabricated on phosphorene exfoliated from black phosphorus and, later, on phosphorene synthesized by using chemical vapor deposition and other material synthesis techniques. To reduce the environmental sensitivity of phosphorene and to explore other novel devices, heterojunctions between phosphorene and graphene, h-BN, MoS_2, or other chalcogenides and oxides would be explored.

What was accomplished towards achieving these goals?

During the project period, phorsphorene field-effect transistors (FETs) were successfully passivated with atomic-layer-deposited (ALD) Al_2O_3 and proven to be stable for at least three months in room air [1], [2]. Meanwhile, the FET design evolved from long back-gated channels on conducting substrates that could be assessed only under direct-current (DC) conditions, to submicron top-gated channels that could operate at microwave frequencies, under both small-signal and large-signal conditions [4], [5]. Further, CMOS-compatible submicron buried-gate structures were designed. However, lacking large-area phosphorene layers, the design was demonstrated only on monolayer MoS_2 grown by chemical vapor deposition [3], [6]. Nevertheless, for the first time, thousands of 2D FETs were batch-processed with high yield, which allowed efficient correlation between device yield/performance and material/process defects. This metrology should help improve the material, design, and process of all 2D FETs in the future.

What opportunities for training and professional development did the project provide?

Four graduate students majoring in electrical engineering were trained through the project. During the project period, one graduated with an MS degree, while another one graduated with a PhD degree.

How were the results disseminated to communities of interest?

In addition to the refereed journal and conference papers listed under **Products** and referenced above, the following presentations and seminars were given at different workshops and academic/industrial/governmental institutions:

J. C. M. Hwang, "Phosphorene MOSFETs–Promising Transistors Based on a few Layers of Phosphorus Atoms," Nanjing Univ. Sci. Tech., Nanjing, China, Mar. 2015.

J. C. M. Hwang, "Phosphorene –Can it be Effectively Passivated?" US-EU Workshop on 2D Layered Materials and Device, Arlington, VA, Apr. 2015.

X. Luo, Y. Rahbarihagh, K. Xiong, J. C. M. Hwang, H. Liu, Y. Du, and P. D. Ye, "Temporal and Thermal Stability of Al_2O_3-Passivated Phosphorene MOSFETs," Graphene and Beyond Workshop, College Park, PA, May 2015.

J. C. M. Hwang, "Phosphorene MOSFETs–Promising Transistors Based on a few Layers of Phosphorus Atoms," U. Texas, El Paso, TX, May 2015.

K. Xiong, X. Luo, and J. C. M. Hwang, "Phosphorene FETs–Promising Transistors Based on a few Layers of Phosphorus Atoms," Air Force Research Lab, Dayton, OH, Jun. 2015.

J. C. M. Hwang, "Phosphorene FETs–Promising Transistors Based on a few Layers of Phosphorus Atoms," National Institute of Standards and Technology, Gaithersburg, Jun. 2015.

J. C. M. Hwang, "Phosphorene FETs–Promising Transistors Based on a few Layers of Phosphorus Atoms," Chinese Academy of Engineering, Chengdu, China, Jul. 2015.

J. C. M. Hwang, "Phosphorene FETs–Promising Transistors Based on a few Layers of Phosphorus Atoms," U. Sci. Tech. China, Nanjing, China, Jul. 2015.

J. C. M. Hwang, "Phosphorene FETs–Promising Transistors Based on a few Layers of Phosphorus Atoms," Nanjing Electronic Devices Institute, Nanjing, China, Jul. 2015.

J. C. M. Hwang, "Phosphorene FETs–Promising Transistors Based on a few Layers of Phosphorus Atoms," Chinese Academy of Sciences, Shanghai, China, Jul. 2015.

J. C. M. Hwang, "Phosphorene FETs–Promising Transistors Based on a few Layers of Phosphorus Atoms," IHP Microelectronics, Frankfurt (Oder), Germany, Sep. 2015.

J. C. M. Hwang, "Phosphorene FETs–Promising Transistors Based on a few Layers of Phosphorus Atoms," U.S.-Korea Forum on Nanotechnology, Arlington, VA, Oct.2015.

J. C. M. Hwang, "Surface Passivation and RF Characterization of Phosphorene FETs," Air Force Research Lab, Dayton, OH, Nov. 2015.

J. C. M. Hwang, "Phosphorene Transistors–Transient or Lasting Electronics?" Workshop Frontier Electronics, San Juan, PR, Dec. 2015.

J. C. M. Hwang, "Phosphorene FETs–Promising Transistors Based on a few Layers of Phosphorus Atoms," Rice U., Houston, TX, Jan. 2016.

K. Xiong, "Phosphorene FET," IHP Microelectronics, Frankfurt (Oder), Germany, Feb. 2018.

J. C. M. Hwang, "Phosphorene FETs–Promising Transistors Based on a few Layers of Phosphorus Atoms," Graphene and Beyond Workshop, College Park, PA, May 2016.

J. C. M. Hwang, "Phosphorene Transistors–A Brief Review," Electrochemical Soc. Meet., San Diego, CA, May 2016.

J. C. M. Hwang, "Phosphorene Transistors–Promising Transistors Based on a few Layers of Phosphorus Atoms," Marche Polytechnic U., Ancona, Italy, Jul. 2016.

J. C. M. Hwang, "Phosphorene FET–New Microwave Transistor Based on a few Layers of Phosphorus Atoms," IEEE MTT-S Int. Microwave Workshop Series Advanced Materials Processes, Chengdu, China, Jul. 2016.

J. C. M. Hwang, "Phosphorene FET–New Microwave Transistor Based on a few Layers of Phosphorus Atoms," Bangor U., Bangor, UK, Oct. 2016.

J. C. M. Hwang, "Phosphorene FET–A Promising Transistor Based on a few Layers of Phosphorus Atoms," U. Southern California, Los Angeles, CA, Nov. 2016.

K. Xiong, L. Li, J. C. M. Hwang, A. Goritz, M. Wietstruck, and M. Kaynak, "Black Phosphorus MOSFETs and CMOS Integration," Muju Int. Winter School, Muju, Korea, Feb. 2017.

J. C. M. Hwang, "Black Phosphorus Field-Effect Transistors–A Brief Review," Muju Int. Winter School, Muju, Korea, Feb. 2017.

J. C. M. Hwang, "Black Phosphorus Field-Effect Transistors–A Brief Review," Korean Inst. Sci. Tech., Seoul, Korea, Feb. 2017.

J. C. M. Hwang, "Assessment of Phosphorene Field-Effect Transistors," ONR Electromagnetic Materials Program 6.1 Peer Review, Arlington, VA, Jun. 2017.

J. C. M. Hwang, "2D-CMOS Integration," AFOSR GHz-THz Electronics Review, Arlington, VA, Jul. 2017.

K. Xiong, L. Li, J. C. M. Hwang, M. Chuang, Y. H. Lee, A. Göritz, M. Wietstruck, and M. Kaynak, "Large-scale CMOS-compatible Processing of MoS2 MOSFETs," Cornell Nanofabrication Facility Annual Meet., Ithaca, NY, Sep. 2017.

J. C. M. Hwang, "Toward 2D-CMOS Integration," US-EU 2D Workshop, Arlington, VA, Oct. 2017.

J. C. M. Hwang, "2D-CMOS Integration," IEEE- MTT-25 RF Nanotechnology / IHP Workshop, Frankfurt (Oder), Germany, Oct. 2017.

J. C. M. Hwang, "Toward 2D-CMOS Integration," U. Bundeswehr, Munich, Germany, Oct. 2017.

K. Xiong, L. Li, R. J. Marstell, X. Luo, A. Madjar, N. C. Strandwitz, J. C. M. Hwang, H. Kim, J.-H. Park, Y. Lee, A. Göritz, C. Wipf, M. Wietstruck, and M. Kaynak, "CMOS-compatible Batch Processing of Monolayer MoS2 MOSFETs," NSF EFRI-2DARE, DMREF-2D, and MIP Grantees Meet., University Park, PA, Nov. 2017.

J. C. M. Hwang, "Toward 2D-CMOS Integration," Taiwan Semiconductor Manufacturing Co., Hsinchu, Taiwan, Dec. 2017.

Important Lessons Learned

<u>Instability of phosphorene makes phosphorene transistors difficult to manufacture.</u>

Although once successfully fabricated and passivated, we have proven that phosphorene transistors could be very stable in room atmosphere [1], the process was very tricky and the yield was very low.

Additionally, to date all phosphorene transistors have been fabricated on layers exfoliated from bulk black phosphorus, and no one has succeeded in synthesizing large-area uniform layers of phosphorene under reasonable pressure and temperature. This raises serious doubt that phosphorene transistors will ever be manufacturable.

Fragility of 2D layers makes it difficult to be coated with high-quality gate insulator.

We have learned that not only phosphorene, other 2D layers such as MoS_2 are also rather fragile. The fragility of 2D layers limit the conditions under which they can be coated with high-quality gate insulator with low interface density for high-performance top-gated MOSFETs. For example, in the case of phosphorene transistors, the temperature of atomic layer deposition (ALD) of Al_2O_3 gate insulator was limited to 200 °C, as opposed to 300 °C necessary for high-quality ALD. Although the quality of the gate insulator could be improved by post-deposition annealing [1], the process remains tricky. To overcome such difficulty, we have evolved from back-gated MOSFETs for DC performance, to top-gated MOSFETs for RF performance, and, finally, to buried-gate MOSFETs for improved RF performance [3], [6]. Although a buried gate is technically also a back gate, it differs from the traditional back gate which utilized the entire Si substrate as the gate. Rather, the buried gate can be of submicron dimension embedded in an insulator such as SiO_2. The surface of the buried gate is made even with the surrounding SiO_2 by chemo-mechanical polishing, and ready for deposition of high-quality gate insulator before any 2D layers are transferred or grown on top. Lacking large-area synthesized phosphorene, we demonstrated such "gate insulator before 2D layer" approach on CVD monolayer MoS_2, which yielded thousands of high-performance MOSFETs and allowed statistical evaluation of device uniformity as well as correlation with material defects [3], [6].

Difficulty in phosphorene fabrication makes $PtSe_2$ more attractive

We have experienced four generations of 2D layers for high-performance transistors: 1) graphene with high mobility but no bandgap, 1) MoS_2 with sizable bandgap but low mobility, 3) phosphorene with sizable bandgap and high mobility, but low stability, and 4) $PtSe_2$ with sizable bandgap, high mobility, and high stability. Although $PtSe_2$ is even newer than phosphorene, large-area $PtSe_2$ has already been synthesized by CVD, molecular beam epitaxy, and direct thermal conversion. Another advantage of $PtSe_2$ is that it is a semiconductor only when it is one or two atomic layers. Thicker $PtSe_2$ is semi-metallic like graphene, which should help overcome the contact problem of most 2D FETs.

Participants

PI, James Hwang, 3 months during the three-year project period.

Students

Number of undergraduate and graduate STEM participants: 4
Number of participants that received a STEM degree: 2

Products

Refereed Journal Papers

[1] X. Luo, Y. Rahbarihagh, J. C. M. Hwang, H. Liu, Y. Du, and P. D. Ye, "Temporal and thermal stability of Al_2O_3-passivated phosphorene MOSFETs," *IEEE Electron Device Lett.*, vol. 35, no. 12, pp. 1314–1316, Dec. 2014. DOI: 10.1109/LED.2014.2362841. Keywords: Elemental semiconductors, high-k gate dielectrics, semiconductor-insulator interfaces, thermal stability, two-dimensional hole gas.

[2] Z. Lin, A. McCreary, N. Briggs, S. Subramanian, K. Zhang, Y. Sun, X. Li, N. Borys, H. Yuan, S. Fullerton-Shirey, A. Chernikov, H. Zhao, S. McDonnell, A. Lindenberg, K. Xiao, B. LeRoy, M. Drndic, J. C. M. Hwang, J. Park, M. Chhowalla, R. Schaak, A. Javey, M. Hersam, J. Robinson, and M. Terrones, "2D materials advances: From large scale synthesis and controlled heterostructures to improved characterization techniques, defects and applications," *2D Matr.*, vol. 3, no. 4, pp. 1–38, Dec. 2016. DOI: 10.1088/2053-1583/3/4/042001. Keywords: 2D materials, transition metal dichalcogenides, review.

[3] K. Xiong, H. Kim, R. J. Marstell, A. Göritz, C. Wipf, L. Li, J.-H. Park, X. Luo, M. Wietstruck, A. Madjar, N. C. Strandwitz, M. Kaynak, Y. H. Lee, and J. C. M. Hwang, "CMOS-compatible batch processing of monolayer MoS2 MOSFETs," *J. Phys. D: Appl. Phys.* Keywords: chemical vapor deposition, CMOS process, MOSFET, semiconductor device manufacture, semiconductor nanostructures, thin film transistors, wafer scale integration. Submitted for publication.

Refereed Conference Papers

[4] K. Xiong, X. Luo, and J. C. M. Hwang, "Phosphorene FETs – Promising transistors based on a few layers of phosphorus atoms," in *IEEE MTT-S IMWS-AMP*, Suzhou, China, Jul. 2015, pp. 1–3. DOI: 10.1109/LED.2014.2362841. DOI: 10.1109/IMWS-AMP.2015.7324944. Keywords: Contacts, dielectric films, MOSFETs, passivation, stability.

[5] X. Luo, K. Xiong, J. C. M. Hwang, Y. Du, and P. Ye, "Continuous-wave and transient characteristics of phosphorene microwave transistors," in *IEEE MTT-S Int. Microwave Symp. (IMS)*, San Francisco, CA, May 2016, pp. 1–3. DOI: 10.1109/MWSYM.2016.7540290. Keywords: Elemental semiconductors, microwave transistors, high-K gate dielectrics, semiconductor-insulator interfaces, hysteresis, photoconductivity.

[6] K. Xiong, L. Li, A. Madjar, J. C. M. Hwang, Z. Lin, Y. Huang, X. Duan, A. Göritz, M. Wietstruck, and M. Kaynak, "Large-scale fabrication of RF MOSFETs on liquid-exfoliated MoS2," in *European Microwave Conf. (EuMC)*, Madrid, Spain, Sep. 2018, pp. 1–4. Keywords: Electrochemical process, CMOS process, MOSFET, semiconductor device manufacture, semiconductor nanostructures, thin film transistors, wafer scale integration. Submitted for publication.